UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/048,932	03/26/1998	DEAN A. KLEIN	MEI-97-01386	4878

7590 05/07/2003

JOSEPH A. WALKOWSKI
TRASKBRITT, PC
P.O. BOX 2550
SALT LAKE CITY,, UT 84110

EXAMINER	
LO, LINUS H	

ART UNIT	PAPER NUMBER
2614	

DATE MAILED: 05/07/2003

23

Please find below and/or attached an Office communication concerning this application or proceeding.

6

Office Action Summary	Application No.	Applicant(s)	
	09/048,932	KLEIN, DEAN A.	
	Examiner	Art Unit	
	Linus H Lo	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2003, Pre-Amend and RCE* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-16 and 18-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-16 and 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 1998* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/19/2003 has been entered.

2. It is noted that the instant application does not explicitly describe "the north bridge" in any specific definition or description , thus it is considered for art rejection purpose, the claimed " north bridge chip" is interpreted as "a logic chip" that has the equivalent function as the described core logic unit on page 5, lines 12-13

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-5, 7, 10, 12, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dea '208 in view of So '559(all of record) .

Considering claim 1(Four-times Amended) Dea discloses a device relating to the field of video processing and in particular, to the compression and decompression of video signals. Dea discloses the following subject matter, note:

a) the claimed apparatus for assisting in compressing video data in a computer system including a central processing unit and a system memory which is met by the video processing system 100 (column 4, lines 17-41, and Fig. 1), whereas the video processor 110 and the DRAM 114 are considered as central processing unit an system memory respectively;

b) the claimed video input port, for receiving video data for a current video frame which is met by bus interface 200 (FIG. 2, column 6, lines 42-44);

c) the claimed video input buffer coupled to the video input port , for storing video data from the video input port which is met by the current frame memory 204 (FIG. 2, 3A, and column 6, lines 42-44) ;

d) the claimed previous frame buffer , for storing at least a portion of a previous video frame which is met by previous image memory 206 (FIG. 2, 3A and column 5, lines 38-47), wherein the described previous image block is the previous video frame;

e) the claimed operation unit coupled to the video input buffer and the previous frame buffer, for computing a difference frame from data from the video input buffer and data from the previous frame buffer which is met by the compression/decompression accelerator 120 (FIG. 2, 3A , and column 9, line 57-column 10, line 3), whereas the described frame difference determination by the frame difference block 220 that performs the computing function ;

f) the claimed result buffer coupled to the operation unit , for temporarily buffering the difference frame prior to storing the difference fame in the system memory which is met by the encoded data storage buffer 248 and the DRAM memory 114 (system memory) (FIG. 2, 3A, and column 9, line 57- column 10, line 3, column 15, lines 8-13 and column 10, line 53 - column 11, line 13), whereas the passage bridging from column 9 and 10 describes the frame difference encoding data by the encoder block 246 which is stored in the buffer 248 first, and the passage from columns 10 to 11 further discloses the run/value pair from the encoder 246 are applied to the encoded output circular buffer 332, in which the buffer 332 may located in DRAM 114 that is interfaced with the video processor 112 ; and

g) the teaching of wherein the apparatus configured to operation with in *a core logic unit* of a computer system which as described by the compress/decompression accelerator 120 that includes the function frame difference block 220 (column 6, lines 36-44, and column 5, lines 42-47, and FIG. 1 and 2), where the description at column 5 and Fig. 2 elucidated the compressor/decompressor 120 is a circuitry within the video interface system that interface with the processor 112 to the RAM by way of accelerator bus interface; and

h) the teaching of the apparatus configured to enable the central processing unit to retrieve the difference frame directly from the system via *the core logic unit* for further compression of the video data by the central processing unit which as described at column 11, lines 19-33, whereas the video process having the function to move blocks of data into and out of the memory 114, and while the accelerator 120 carries out the

computational intensive frame adding/subtracting and run length encoding decoding (compression).

However Dea does not explicitly disclose the claimed **apparatus configured to operate within a north bridge chip** of the computer system to enable the central processing unit to retrieve the difference frame directly from the system memory via **the north bridge chip for** further compression of the video data by the central processing unit.

Nonetheless Dea teaches the comprssion/depression accelerator 120 as a core logic unit for a computer system as described above at (g), and the apparatus is configured to enable the central processing unit to retrieve the difference frame directly from the system via *the core logic unit* which as described above at (h) .

So discloses an integrated circuit provides on a single chip for use with a first processor off-chip. So discloses that a VSP (wrapper-and-digital signal processor-core) used as a **graphic accelerator** that is provided either as the North bridge or AGP graphic/video chip as described at column 17, lines 24-43, in which the data after the VSP processing, the data will then be passed out with higher bandwidth. It is noted that So also discloses that accelerator (core logic unit) is provided at the North Bridge chip, and whereas such implementation which has the advantage of achieving MIPS (millions of instructions per second) column 4, lines 14-16, without substantially loading PCI , peripheral component interface bus (column 17, lines 24-32).

Therefore the examiner submits that it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Dea's teaching of video

accelerator (core logic unit) with the teaching of **graphic accelerator** that is implemented as the **North bridge chip** for the stated advantage.

Considering claim 2(Amended) , the claimed memory port coupled to the previous frame buffer and the result buffer, for transferring data to and from the system memory that stores video data from the video input port and result data from the result buffer which is met by bus interface 200 (FIG. 2, column 5, lines 38-47, column 7, lines 39-44 and column 11, lines 19-33), in which the passage from column 5 described that the memory port is coupled to the previous frame buffer, while excerpt from column 7 described the memory port is coupled to the result buffer, whereas the passage from column 11describes the video process having the function to move blocks of data into and out of the memory 114, and while the accelerator 120 carries out the computational intensive frame adding/subtracting and run length encoding decoding (compression).

Considering claim 3(Amended) , the system of Dea and So discloses all the claimed limitations except for the claimed system memory **couples to the memory port** for storing the video data form the video input port and the difference frame from the result buffer, wherein the video data is stored in a current frame area in the system memory and the difference frame is stored in a difference frame area in the memory.

Nonetheless, Dea discloses *a memory for storing the video data form the video input port and difference fame from the result buffer,* wherein the video data is stored in a current frame area in the memory and the difference frame is stored in a difference frame area in the memory 114 (column 10, lines 39-46, and column 11, lines 8-18), in which the excerpt from column 10 discloses that the video data is stored in a current frame area in the memory 114, and the passage from column 11 discloses the difference frame is stored in a difference frame area in the memory 114. As such, a memory port inherently exists with respect to the memory 114 to facilitate the transfer of data to and from the compression /decompression accelerator 120.

Considering claim 4 (Amended) , the system of Dea and So discloses *the buffers* store a current video frame and a previous video frame in the same location in *the buffer memory*, allowing the current video frame to be written over the previous video frame which as described by the description of Dea at column 12, lines 24-44, whereas the described physical buffer memory 350 which originally stores previous image and subsequently a current image is being stored in the same location in physical buffer memory 350.

However, the system does not disclose the use of **system memory** store a current video frame and a previous video frame in the same location in **system memory.**

Nonetheless, Dea discloses that at column 11, lines 8-13 where buffer memory, i.e. encode buffer 332, may be located in memory 114 (system memory).

It is noted that the implementation of system memory RAM to use as the buffer memory which has the benefit of utilizing the same memory element to perform two storage function for maintaining a lower manufacturing cost by using less parts.

Therefore the examiner submits that it would have been obvious to one having ordinary skilled in the art at the time the invention was made to implement **the system memory** to store a current video frame and a previous frame in the same location for the intended advantage as stated above.

Considering claim 5 (Amended) , the system of Dea and So discloses the claimed invention except for the claimed wherein the system memory also stores instructions and data for a central processing unit of a computer system.

Dea teaches *a memory* for the computer system in the memory as the description of DRAM 114 at column 4, lines 52-63, and furthermore Dea teaches that the video processing system 100 (computer system) utilizes executable program instructions (column 4, lines 36-51). Examiner takes Official Notice that it is both notoriously well-known in the art to integrate video processing systems in computer systems, and to consolidate storage for disparate processes in common memories.

Therefore it is submitted that it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the Dea and So accordingly in order to provide a computer backbone to facilitate the video processing, and to make efficient use of memory storage capacity.

Considering claim 7, note:

a) the claimed video input buffer stores a block of data from the video input port is met by the data of current image block 326 (column 6, lines 42-44 and column 10, lines 53-56);

b) the claimed previous frame buffer stores a block of data from the previous video frame is met by previous image block (column 5, lines 38-47);

c) the claimed result buffer stores a block of data from the operation unit is met by the buffer 248 (column 10, lines 53-56, and column 9, line 60- column 10, line 3); and

d) the claimed operation unit performs an operation between a block of data from the video input port and a block of data from the previous frame buffer is met by the description at column 9, line 60- column 10, line 3, where the frame different block 220 is considered as the operation unit.

Considering claim 10, the claimed additional resources within the apparatus, for compressing the video data from the video input port is met by the element in FIG. 2 and description at column 6, lines 36-64, where the compression/decompression accelerator 120 consists of additional resources for the purpose of compression.

Considering claim 20(Four-times Amended), claim 20 recites the same limitations as in claim 1, namely the claimed video input port, the video input buffer, the previous frame buffer, the operation unit and the result buffer and the apparatus as a core logic chip, thus claim 20 is

rejected for the same reason as claim 1 above. Additionally, the claimed central processing unit within the computer system is met by the processor 112 (FIG. 1 and column 4, lines 37-45).

Considering claim 12, the system of Dea and So discloses all the claimed limitation except for the claimed video input buffer being a register that **stores less than one video frame**.

However, smaller storage capacity memory devices have the benefit of more cost efficiency in manufacturing.

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Dea and So teachings accordingly for the stated advantage.

5. Claims 6, and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dea and So and further in view of Abramatic et al. '383 (all of record) .

Considering claim 6, the system of Dea and So discloses the claimed invention except for the claimed limitation of wherein the operation unit performs an exclusive-OR operation between data from the video input buffer and data from the previous frame buffer.

Nonetheless, Dea teaches that the operation unit performs *a computing of the difference frame* between data from the video input buffer and data from the previous frame buffer as discuss above in claim 1.

Additionally, Abramatic et al. teach that a form of compression consists detecting variations (difference) between one image and the next image as described at column 2, lines 53-56. Abramatic et al. discloses the claimed operation unit performs an exclusive-OR operation between data from the video input buffer and data from the previous frame buffer as met by the description at column 6, lines 52-58, whereof the described previous image at the input 55 and the arrival of new points at the input 57 which are respectively considered as the previous and current video frame.

Abramatic et al. teaches that XOR function for the difference calculation 56 which has the advantage of providing a less complicated means for the difference calculation techniques as elucidated at column 7, lines 32-35. Therefore it would have been obvious to one have ordinary skilled in the art at the time the invention was made to modify the Dea and So combination with such teaching for the stated advantage.

Considering claim 13(Four-times Amended), Dea discloses a device relating to the field of video processing and in particular, to the compression and decompression of video signals. Dea discloses the following claimed subject matter, note :

a) the apparatus for compressing video data in a computer system including a central processing unit which is met by the video processing system 100 (column 4, lines 17-41, and Fig. 1), whereas the video processor 110 and the DRAM 114 are considered as central processing unit an system memory respectively;

b) the claimed video input port, for receiving video data for a current video frame is met by bus interface 200 (FIG. 2, column 6, lines 42-44);

c) the claimed video input buffer coupled to the video input port , for storing video data from the video input port is met by the current frame memory 204 (FIG. 2, 3A, and column 6, lines 42-44) ;

d) the claimed previous frame buffer , for storing at least a portion of a previous video frame is met by previous image memory 206 (FIG. 2, 3A and column 5, lines 38-47), wherein the described previous image block is the previous video frame; and

e) the claimed memory port coupled to the previous frame buffer and the result buffer which is met by bus interface 200 (FIG. 2, column 5, lines 38-47, and column 7, lines 39-44), wherein the passage from column 5 described that memory port coupled to previous frame buffer, while excerpt from column 7 described the memory port coupled to result buffer.

However, Dea does not explicitly disclose the following limitations , note:

i) the claimed **exclusive-OR unit** coupled to the video input buffer and the previous frame buffer, for performing an exclusive-OR operation between data from the video input buffer and data from the previous frame buffer;

ii) the claimed result buffer coupled to the **exclusive-OR unit ,** for temporarily buffering the difference frame;

iii) the claimed system memory coupled to the memory port for storing the video data from the video input port and the difference frame from the result buffer, wherein the video data is stored in a current frame in the memory ; and

iv) the claimed apparatus configured to operate within **a north bridge chip** of the computer system to enable the central processing unit to retrieve the difference frame directly from the system memory via **the north bridge chip** for further compression of the video data by the central processing unit.

In regard to (i), Dea teaches that *an operation unit* coupled to the video input buffer and the previous frame for performing *a computing of the difference frame* from the video input buffer and data from the previous frame buffer which as described by the compression/decompression accelerator 120 (FIG. 2, 3A , and column 9, line 57- column 10, line 3), wherein the described frame difference determination by the frame difference block 220 is considered as the operation.

And further in regard to (ii) , Dea teaches that the result buffer coupled to *the operation unit* , for temporarily buffering the difference frame which as described by the encoded data storage buffer 248(332) (FIG. 2, 3A, and column 9, line 57- column 10, line 3, column 15, lines 8-13 and column 10, line 53-column 11, line 7).

Nonetheless, Abramatic et al. teaches that a form of compression consists in detecting variations (difference) between one image and the next image as described at column 2, lines 53-56. Abramatic et al. discloses the claimed exclusive-OR unit , for performing an exclusive-OR operation between data from the video input buffer and data from the previous frame buffer as met by the description at column 6, lines 52-58, in which the described previous

image at the input 55 and the arrival of new points at the input 57 which are respectively considered as the previous and current video frame.

Since Abramatic et al. teach that XOR function for the difference calculation 56 which has the advantage of providing a less complicated means for the difference calculation techniques as elucidated at column 7, lines 32-35. Therefore it would have been obvious to one have ordinary skilled in the art at the time the invention was made to modify the system of Dea with such teachings for the stated advantage.

In regard to (iii), Dea discloses *a system memory for storing the video data form the video input port and result data from the result buffer,* wherein the video data is stored in a current frame area in the memory and the result data is stored in a difference frame area in the memory 114 (column 10, lines 39-46, and column 11, lines 8-18), in which the excerpt from column 10 discloses that the video data is stored in a current frame area in the memory 114, and the passage from column 11 discloses that the result data is stored in a difference frame area in the memory 114. As such, a memory port inherently exists with respect to the memory 114 to facilitate the transfer of data to and from the compression /decompression accelerator 120.

In regard to (iv) , Dea teaches the following , note:

- the limitation of the apparatus configured to operation with in *a core logic unit* of a computer system which as described by the compress/decompression accelerator 120 that includes the function frame difference block 220 (column

6, lines 36-44, and column 5, lines 42-47, and FIG. 1 and 2), where the description at column 5 and Fig. 2 elucidated the compressor/decompressor 120 is a circuitry within the video interface system that interface with the processor 112 to the RAM by way of accelerator bus interface; and

- the limitation of the apparatus configured to enable the central processing unit to retrieve the difference frame directly from the system via *the core logic unit* for further compression of the video data by the central processing unit which as described at column 11, lines 19-33, whereas the video process having the function to move blocks of data into and out of the memory 114, and while the accelerator 120 carries out the computational intensive frame adding/subtracting and run length encoding decoding (compression).

However Dea does not explicitly disclose the claimed **apparatus configured to operate within a north bridge chip** of the computer system to enable the central processing unit to retrieve the difference frame directly from the system memory via **the north bridge chip for** further compression of the video data by the central processing unit.

So discloses an integrated circuit provides on a single chip for use with a first processor off-chip. So discloses that a VSP (wrapper-and-digital signal processor-core) used as a **graphic accelerator** that is provided either as the North bridge or AGP graphic/video chip as described at column 17, lines 24-43, in which the data after the VSP processing, the data will then be passed out with higher bandwidth. It is noted that So also discloses that accelerator (core logic unit) is provided at the North Bridge chip, and whereas such implementation which has

the advantage of achieving MIPS (millions of instructions per second) column 4, lines 14-16, without substantially loading PCI , peripheral component interface bus (column 17, lines 24-32).

Therefore the examiner submits that it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Dea's teaching of video accelerator (core logic unit) with the teaching of **graphic accelerator** that is implemented as the **North bridge chip** for the stated advantage.

Considering claim 14 (Amended) , the system of Dea and So discloses *the buffers* store a current video frame and a previous video frame in the same location in *the buffer memory*, allowing the current video frame to be written over the previous video frame which as described by the description of Dea at column 12, lines 24-44, whereas the described physical buffer memory 350 which originally stores previous image and subsequently a current image is being stored in the same location in physical buffer memory 350.

However, the system does not disclose the use of **system memory** store a current video frame and a previous video frame in the same location , allowing the current video frame to be written over the previous video frame.

Nonetheless, Dea discloses that at column 11, lines 8-13 where buffer memory, i.e. encode buffer 332, way be located in memory 114 (system memory).

It is noted that the implementation of system memory RAM to utilize also as the buffer memory which has the benefit of utilizing the same memory element to perform two storage function for maintaining a low cost implementation .

Therefore the examiner submits that it would have been obvious to one having ordinary skilled in the art at the time the invention was made to implement **the system memory** to store a current video frame and a previous frame in the same location for the intended advantage as stated above.

Considering claim 15 (Amended) , the system of Dea, So and Abramatic et al. discloses the claimed invention except for the claimed limitation wherein the system memory stores **instructions and data** for the central processing unit of the computer system.

Dea teaches *a system memory* for the computer system as the description of DRAM 114 at column 4, lines 52-63, and furthermore Dea teaches that the video processing system 100 (computer system) utilizes executable program instructions (column 4, lines 36-51). Examiner takes Official Notice that it is both notoriously well-known in the art to integrate video processing systems in computer systems, and to consolidate storage for disparate processes in common memories.

Therefore it is submitted that it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the system of Dea, So and Abramatic et al. accordingly in order to provide a computer backbone to facilitate the video processing, and to make efficient use of memory storage capacity.

Considering claim 16 (Amended) , note:

a) the claimed video input buffer stores a block of data from the video input port is met by the data of current image block 326 of Dea (column 6, lines 42-44 and column 10, lines 53-56);

b) the claimed previous frame buffer stores a block of data from the previous video frame is met by previous image block of Dea (column 5, lines 38-47);

c) the claimed result buffer stores a block of data from the exclusive-OR unit which is met by the buffer 248 of Dea (column 10, lines 53-56, and column 9, line 60- column 10, line 3) and the obviousness discussion as presented in claim 13 point (ii) ; and

d) the claimed exclusive-OR unit performs an exclusive-OR operation between a block of data from the video input port and a block of data from the previous frame buffer is met by the description of difference calculator performs an X-OR function at column 6, lines 52-58 of Abramatic et al., whereof the described previous image at the input 55 and the arrival of new points at the input 57 which are respectively considered as the previous and current video blocks.

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dea ' 208 and So '559 in view of Yan '374 (all of record) .

Considering claim 9, the system of Dea and So discloses all the claimed limitation except for the claimed wherein the apparatus comprises part of a video conferencing system .

Nonetheless Dea teaches a compressed video data is being generated and utilized from the disclosed compression/decompression accelerator 120 as described at column 4, line 17-22. Additionally, Yan teaches the generated compressed video signal that is commonly having the application in videophone, video conference and other audio-visual transmission over networks as described at column 3, lines 52-64.

The examiner submits that it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the compressed video data scheme as part of a video conference system in order to facilitate the benefit of bandwidth conservation in video data transmission.

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dea '208 and So '559 in view of Hardiman ' 223 (all of record) .

Considering claim 11, the system of Dea and So discloses all the claimed limitations except for the claimed color space conversion circuit coupled between the video input port and the video input buffer.

Hardiman discloses an invention which relates to compression coding of a video program. Hardiman discloses the claimed color space conversion circuit coupled between the video input port and the video input buffer is met by the subsampler and color space converter 80 (column 3, lines 47-57, column 6, lines 55-64, and FIG. 2), where the described video data/bus and the subsample FIFO are considered as the video input port and buffer, respectively.

Hardiman discloses that by implementing the color space conversion on video data

provides the benefit of properly converting the video information from a computer processed information into a displayable signal for image displaying (column 3, lines 47-57).

The examiner submits that it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Dea and So by using the color space conversion circuit as taught by Hardiman for the stated benefit.

8. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over the system of Dea, So and Abramatic et al. as applied to claim 13 above, and further in view of Yan '374 (all of record) .

Considering claim 18, the system of Dea, So and Abramatic et al. discloses all the claimed limitations except for the claimed wherein the apparatus comprises part of a video conferencing system .

Nonetheless Dea teaches a compressed video data is being generated and utilized from the disclosed compression/decompression accelerator 120 as described at column 4, line 17-22. Additionally Yan teaches the generated compressed video signal that is commonly having the application in videophone, video conference and other audio-visual transmission over networks as described at column 3, lines 52-64.

The examiner submits that it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the compressed video data scheme as part of a video conference system in order to facilitate the benefit of bandwidth conservation in video data transmission.

9. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over the system of Dea, So and Abramatic et al. as applied to claim 13 above, and further in view of Hardiman ' 223 (all of record) .

Considering claim 19, the system of Dea, So and Abramatic et al. discloses all the claimed limitations except for the claimed **color space conversion circuit** coupled between the video input port and the video input buffer.

Hardiman discloses an invention which relates to compression coding of a video program. Hardiman discloses the claimed color space conversion circuit coupled between the video input port and the video input buffer is met by the subsampler and color space converter 80 (column 3, lines 47-57, column 6, lines 55-64, and FIG. 2), where the described video data/bus and the subsample FIFO are considered as the video input port and buffer, respectively.

Hardiman discloses that by implementing the color space conversion on video data provides the benefit of properly converting the video information from a computer processed information into a displayable signal for image displaying (column 3, lines 47-57).

The examiner submits that it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Dea, So and Abramatic et al. by using the color space conversion circuit as taught by Hardiman for the stated benefit.

Response to Arguments

10. Applicant's arguments filed 2/19/03 have been fully considered but they are not persuasive.

a) Applicant argues that Dea teaches away from storing the data in the system memory by disclosing that "accelerator 120 of Dea present invention within remote video interface system has a straight pipeline architecture rather than shared resources ."

b) Applicant argues that So engages in additional compression/decompression complexity within the North bridge and does not disclose "computing the difference frame in the core logic chip ...; storing the difference ....via the core logic chip to complete compression of the video data." as claimed by Applicants in amended independent claim 1. Therefore, Applicants respectfully request that the rejection to claim 1, be withdrawn.

c) Applicant argues that regarding claims 2-5, 7, 10 and 12, each of claims includes additional element and depending either directly or indirectly from amended independent claim 1, each of these claims, as a whole, distinguish over the cited references. Therefore , Applicants respectfully request that the rejections to claims 2-5, 7, 10 and 12 be withdrawn.

d) Regarding claim 20, Applicant argues that Dea and So do not appear to teach or suggest a computer system for "computing ... central processing unit", as claimed by Applicants. See the arguments above with reference to claim 1.

e) Regarding claim 6, Dea, So and Abramatic , either individually , or in any proper combination , do not teach, suggest, or motivate Applicants' invention of claim 6. Applicants sustain the arguments above that noting within the four corners of the cited references teach each and every element of Applicants' invention as claimed, including the elements of the base claim from which claim 6 depends.

f) Regarding claims 13-16, Dea, So, and Abramatic, either individually or in any proper combination, do not teach, suggest or motivate Applicants' invention of claims 13-16. Applicant sustain the arguments about that nothing within the cited references teach each and every element of Applicants' invention as claimed in amended claim 13 and claims 14-16 depending thereform.

g) Regarding claim 9, Dea, So and Yan either individually , or in any proper combination, do not teach, suggest or motive Applicants' invention as claim 9, including all of the claim limitations of the base claim. ... In support , Applicant sustain the argument above as applied to the base claim, amended independent claim 1.

h) Regarding claim 11, Applicants sustain the arguments above as applied to the base claim. Therefore, since Dea, So or Hardiman, either individually or in any proper combination, do not teach , suggest , or motivate Applicants' inventions as claimed in claim 11, and further in view of the claim taken as a whole and the whole and the

novelty associated therewith, Applicants respectfully request that rejection to claim 11 be withdrawn.

i) Regarding claim 18, Dea, So, Abramatic, and Yan either in any proper combination, do not teach, suggest or motive Applicants' invention as claim 18, including all of the claim limitations of the base claim. ... In support , Applicant sustain the argument above as applied to the base claim, Therefore, since Dea, So or Yan , either individually or in any proper combination, do not teach , suggest , or motivate Applicants' inventions as claimed in claim 18, and further in view of the claim taken as a whole and the whole and the novelty associated therewith, Applicants respectfully request that rejection to claim 18 be withdrawn.

j) Regarding claim 19, Dea, So, Abramatic, and Yan either in any proper combination, do not teach, suggest or motive Applicants' invention as claim 19, including all of the claim limitations of the base claim. ... In support , Applicant sustain the argument above as applied to the base claim, Therefore, since Dea, So or Yan , either individually or in any proper combination, do not teach , suggest , or motivate Applicants' inventions as claimed in claim 19, and further in view of the claim taken as a whole and the whole and the novelty associated therewith, Applicants respectfully request that rejection to claim 19 be withdrawn.

Examiner Response

a), d), e) Examiner disagrees. It is noted that Dea teaches the accelerator 120 within remote video interface system that has a straight pipeline architecture rather than shared resource which as taught at column 5, lines 25-27. However, it does not restrict the accelerator 120 or the processor 112 to utilize the DRAM 114(system memory) of the system that is external to the processor 112 or accelerator 120. In support, the passage from column 9 , line 65- column 10, line 11, and Fig. 2, whereas the passage describes that the accelerator 120 (core logic unit) includes blocks 238, 246 that perform further encoding operation and stores the encoded data in buffer 248. Furthermore, passage from column 11, lines 5-13, which additionally teaches that the data as run/value pair for run length encoder 246 are applied by way of line 330 to encode output circular buffer 332. The data within encode output circular buffer 332 is then applied to variable length encoder 112b. The buffer 332 is being understood that may be located in memory 114 in order to perform the operations of variable length encoder 112b. Therefore the above excerpt has clearly demonstrated that the storing of the different frame (encoded data frame) in the system memory (memory 114). Thus applicant argument is deemed not persuasive and the art rejection is maintained.

b) In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). It is noted that the reference of So is introduced for demonstrating the obviousness of

facilitating the North bridge chip in the system of Dea, whereas rather difference as contended by the applicants for the lacking disclosure. Thus the applicant is not persuasive.

c), f)-j) Since applicant does not present any additional argument concerning the art rejection and contends the dependents claims includes additional element and depending to the allowable independent claim. Thus no further argument is deemed necessary in view of the examiner response as for based independent claims above.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linus H. Lo whose telephone number is (703) 305-4039.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John W. Miller, can be reached at (703) 305-4795.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

lhl L L

MICHAEL H. LEE
PRIMARY EXAMINER

April 28, 2003